REMARKS

The present amendment is responsive to the Official Action mailed November 1, 2002. A petition for a three-month extension of time to respond to the Official Action, to and including May 1, 2003 is submitted herewith, together with a copy thereof.

Claims 1, 8-9, 15 and 17 stand rejected under 35 U.S.C. § 102(e) hereinafter as being anticipated by U.S. Patent No. 6,098,282 to *Frankeny et al.* ("*Frankeny*") Claims 2, 4-7, 10-14, 16, 18-19, 22, 25-31, and 33-34 stand rejected under 35 U.S.C. § 103 as being obvious over *Frankeny* alone, or in combination with one or more other references, or official notice. Claims 3, 20-21, 23-24, and 32 are currently withdrawn from consideration. Reconsideration and withdrawal of the rejections is respectfully requested, in view of the following comments.

As amended, the two independent claims of the application, claims 1 and 28, recite methods of making a multi-layer circuit assembly having metallic via liners which connect the outer metal layers of the multi-layer circuit assembly, but which are insulated from the first and second metal layers which lie therebelow. Because some of the metallic via liners are insulated from the first and second metal layers, they can provide connections between patterns in the first and second outer metal layers without having to connect to one or both of the first and second metal layers in the interior of the structure. Support for the amendments is provided, inter alia, at page 4, lines 21 to 23; page 5, lines 3-6; and at page 5, lines 14-17 of the Specification. In particular, page 6, lines 12-14 of the Specification states that:

> at least some of said signal lines are connected to said first and second metal layers,

indicating that other signal lines are not connected to

said first and second metal layers, and are therefore electrically isolated from the first and second metal layers.

Frankeny neither teaches nor suggests these features of claims 1 and 28, neither alone, nor in combination with the other references cited by the Examiner to reject the claims. Rather, *Frankeny* teaches precisely the opposite. *Frankeny* teaches a multi-layer structure in which outer metal layers 42 and 43 (Figure 19 of *Frankeny*) are, in fact, purposely connected to a first interior metal layer 26 through an opening 39 in a dielectric layer, and to the second metal layer 29 through another opening 41 in a dielectric layer, to form capacitor structures including the first and second metal layers 26, 29 of the interior (col. 6, lns. 55–65). Moreover, none of the other references cited by the Examiner to reject these claims teach or suggest these features. Since all other claims of the application depend from claims 1 and 28, the rejection of all claims should be withdrawn.

Claims 2, 4-7, and 10-12 stand rejected under 35 U.S.C. § 103(a) as being obvious over *Frankeny*, in view of U.S. Patent No. 6,378,201 to *Tsukada et al.* (hereinafter, "*Tsukada*"). First, and perhaps, most important of all, is the distinction between the field to which *Frankeny* is directed, namely, the fabrication of thin film capacitors, and *Tsukada*, which is directed to the fabrication of printed wiring boards. These fields have obviously very different goals, and very different concerns. For example, in the field to which *Frankeny* relates, the fabrication of capacitors, it is desirable to maximize an area A of a conductive plane, maximize the dielectric constant k, while minimizing the distance d between conductive planes, in order to achieve maximum capacitance C within a given volume, according to the relation:

$$C = kA/d.$$

On the other hand, the field of *Tsukada*, which relates to

printed wiring boards, has very different goals, in that capacitance is generally an undesirable result. Hence, it is generally sought to provide a dielectric layer between signal planes of a printed wiring board that has at least a minimum required thickness, in order to reduce parasitic capacitance. Moreover, the dielectric constant k and the area A over which particular signal conductors face each other may also be minimized, in order to further such goals. Because *Frankeny* and *Tsukada* are directed to such obviously different fields, they are not properly combinable as references. One skilled in the art of fabricating printed wiring boards would not normally look to a reference relating to the fabrication of capacitors such as *Frankeny*.

The Examiner asserts that claims reciting that signal lines of the first and second outer metal layers are perpendicular to each other are disclosed in *Tsukada* by a combination of horizontal signal lines in the plane of the wiring level and vertical signal lines in the vias. In further distinction from *Tsukada*, claim 2 is amended herein to recite that signal lines formed in each of the outer metal layers are substantially parallel to the planes of the first and second metal layers, respectively. In such way, the recitation of claim 3 that the first signal lines are perpendicular to the second signal lines more clearly refers to perpendicular directions within these substantially parallel planes of the first and second outer metal layers. *Tsukada* neither teaches nor suggests such an arrangement. Support for these amendments are provided at page 11, 5-7 and page 12, lines 19-28, among others.

Moreover, claim 7 recites a method that is clearly neither taught nor suggested by *Frankeny*, alone or in combination with *Tsukada*. Claim 7 recites that additional signal lines are formed (in addition to the signal lines formed in the

outer metal layers, as recited in claim 2), in at least one of the first and second metal layers before the coating step. Clearly, *Frankeny* lacks this feature, as the interior metal layers 26 and 32 (also referenced sometimes as "29") therein are patterned to form only conductive capacitor plates, not signal lines (col. 6, 30-37, and col. 6, line 66 through col. 7, line 5). *Tsukada* does not provide the teachings that *Frankeny* lacks. In *Tsukada* there is no step of coating the first and second metal layers and through vias with a dielectric material, as set forth in claim 1, from which claim 7 ultimately depends. Rather, *Tsukada* teaches that through holes are drilled, and then directly plated with a metal, without first providing a dielectric coating over the structure and in the holes (col. 3, lns. 38-50). Consequently, *Tsukada* clearly fails to teach or suggest this feature.

Claims 13-14 were rejected under 35 U.S.C. § 103(a) as being obvious over *Frankeny* and *Tsukada*, in view of U.S. Patent No. 4,834,835 to *Cziep et al.* (hereinafter, "*Cziep*"). Despite the Examiner's assertion that *Cziep* discloses plasma dry etching of via through holes after laser drilling, there is no such teaching or suggestion therein. *Cziep* merely describes plasma dry etching of an article after photoresist patterning to form the via itself. Unlike claim 14 of the present application in which plasma dry etching is recited as being used to remove dielectric material remaining in the via after the laser patterning, *Cziep* teaches that the dielectric glass fiber of the plastic sheet should be left in place as a desired result (col. 4, lns. 52-58).

Claim 22 was rejected under 35 U.S.C. § 103(a) as being obvious over *Frankeny*, in view of Official Notice. This rejection is traversed. As set forth in claim 22, the first and second metal layers are etched, while the inner dielectric element is laser drilled, to form through vias. *Frankeny*

describes chemically etching the "capacitor core sheet" by etching the metal layers together with the inner dielectric element to form via holes (col. 6, lns. 43-45). *Frankeny* teaches that the etching process is appropriate, given that the thickness of the inner dielectric element is 0.001 mm (i.e. 1 micron)(col. 5, lns 48-51).

However, claim 22 recites that laser drilling of the inner dielectric element is performed after etching the first and second metal layers. Contrary to the Examiner's assertion, one would not normally consider combining a reference such as *Frankeny*, which deals with etching a dielectric layer of 1 micron thickness together when etching outer metal layers, with teachings regarding laser drilling, because of the inefficiency of unnecessarily switching processes and the potential problems in laser drilling, in context of such a thin dielectric layer as in *Frankeny*. Therefore, this rejection should be withdrawn.

The rejection of claim 27 presents a similar issue. Claim 27 was rejected under 35 U.S.C. § 103(a) as being obvious over *Frankeny*. Claim 27 recites that the inner dielectric element is approximately 25-50 microns thick. By contrast, *Frankeny* teaches an inner dielectric element having a 0.001 mm (1 micron) thickness (col. 5, lns. 48-51). As pointed out above, and as reinforced in claim 27, the presently claimed invention and *Frankeny* clearly relate to different fields, the presently claimed invention providing a method of making a multi-layer circuit assembly, and *Frankeny* teaching a method of fabricating a capacitor structure. The recitation in claim 27 of the much greater thickness of the dielectric element only serves to highlight that distinction, the much thicker dielectric element recited in claim 27 providing a surface on which first and second metal layers of the claimed multi-layer circuit assembly are formed. Thus, *Frankeny* is improperly applied to claim 27, and the rejection should be withdrawn.

The remaining rejections of claims 16, 18-19, 25-26, 28-31 and 33-34 should be withdrawn based on the above comments relative to claims 1 and 28, from which these claims depend.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version With Markings to Show Changes Made**".

As it is believed that all of the rejections set forth in the Official Action have been fully met, favorable reconsideration and allowance are earnestly solicited.

If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that he telephone applicant's attorney at (908) 654-5000 in order to overcome any additional objections which he might have.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge Deposit Account No. 12-1095 therefor.

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Respectfully submitted,

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Version With Markings to Show Changes Made

In the Claims:

1. (Amended) A method of making a multi-layer circuit assembly comprising the steps of:

(a) providing a core structure including an inner dielectric element having first and second metal layers on opposite surfaces thereof;

(b) forming one or more through vias extending through said metal layers and said inner dielectric element;

(c) coating said metal layers and said through vias with a dielectric material to thereby form a coated structure having first and second outer dielectric layers overlying the first and second metal layers respectively and dielectric material lining said through vias;

(d) providing outer metal layers over said first and second outer dielectric layers;

(e) metallizing said coated through vias to form metallic via liners connecting said outer metal layers and insulated from said first and second metal layers; and

(f) patterning said outer metal layers such that at least some of said metallic via liners are electrically isolated from said first and second metal layers.

2. (Amended) ~~A~~ The method as claimed in claim 1 ~~further comprising the step of selectively~~ wherein said patterning of said outer metal layers ~~to form~~forms first signal lines overlying and substantially parallel to the plane of said first metal layer and second signal lines overlying and substantially parallel to the plane of said second metal layer.

4. (Twice Amended) ~~A~~ The method as claimed in claim 2, wherein

said first signal lines are substantially perpendicular to said second signal lines.

5. (Amended) ~~A~~ The method as claimed in claim 1 further comprising the steps of forming blind vias through said outer dielectric layers to expose one or more regions of said first and second metal layers and metallizing said blind vias so that at least some of said signal lines are connected to said first and second metal layers.

6. (Amended) ~~A~~ The method as claimed in claim 5 wherein said steps of metallizing said blind vias and metallizing said through vias are performed simultaneously.

7. (Amended) ~~A~~ The method as claimed in claim 2, further comprising the step of forming additional signal lines in at least one of said first and second metal layers before the coating step.

8. (Amended) ~~A~~ The method as claimed in claim 1, wherein each said through via has side walls, said side walls being covered by said dielectric material during the coating step.

9. (Twice Amended) ~~A~~ The method as claimed in claim 2, wherein the selectively patterning step includes the step of selectively removing portions of the outer metal layers.

10. (Amended) ~~A~~ The method as claimed in claim 9 wherein the selectively patterning step includes the step of selectively etching the outer metal layers to form said first and second signal lines therein.

11. (Amended) ~~A~~ The method as claimed in claim 5, wherein the

step of providing outer metal layers over the first and second outer dielectric layers includes the step of:

depositing a seed layer over said outer dielectric layers including the blind vias and the exposed regions of said first and second metal layers;

plating or sputtering a metal onto said seed layer.

12. (Amended) ~~A~~ The method as claimed in claim 2 wherein said step of selectively patterning said outer metal layers includes the step of selectively depositing said outer metal layers.

13. (Amended) ~~A~~ The method as claimed in claim *5*, wherein the step of forming said blind vias includes the step of laser drilling said outer dielectric layers.

14. (Amended) ~~A~~ The method as claimed in claim 13, further comprising the step of plasma etching said blind vias after the laser drilling step to remove any said dielectric material residue remaining in said blind vias.

15. (Amended) ~~A~~ The method as claimed in claim 1, wherein during the coating step said dielectric material is provided having a uniform thickness.

16. (Amended) ~~A~~ The method as claimed in claim 1, wherein after the coating step said dielectric material has a uniform thickness of approximately 25-75 microns.

17. (Amended) ~~A~~ The method as claimed in claim 1, wherein after the coating step said through vias remain open.

18. (Amended) ~~A~~ The method as claimed in claim 1, wherein said through vias have a diameter of approximately 175-200 microns

before the coating step and approximately 25-150 microns after the coating step.

19. (Amended) ~~A~~ The method as claimed in claim 1, wherein the coating step includes the step of electrophoretically depositing said dielectric material.

22. (Amended) ~~A~~ The method as claimed in claim 1, wherein the step of forming said through vias includes the steps of etching said first and second metal layers and drilling said inner dielectric element.

25. (Amended) ~~A~~ The method as claimed in claim 1, wherein the step of forming said through vias includes the steps of:

etching said first and second metal layers to provide aligned openings therein;

aligning a laser in one of said aligned openings and drilling said inner dielectric element.

26. (Amended) ~~A~~ The method as claimed in claim 1, wherein said first and second metal layers are approximately 1-18 microns thick.

27. (Amended) ~~A~~ The method as claimed in claim 1, wherein said inner dielectric element is approximately 25-50 microns thick.

28. (Three Times Amended) A method of making a multi-layer circuit assembly comprising the steps of:

(a) providing an inner dielectric element;

(b) providing first and second metal layers having openings therein on opposite surfaces of said inner dielectric element, said openings defining edges in said first and second metal layers, each said

opening in said first metal layer being in substantial alignment with one of said openings in said second metal layer;

(c) coating said inner dielectric element and said first and second metal layers and said edges of said first and second metal layers with a dielectric material to thereby form a coated structure having first and second outer dielectric layers covering ~~the~~ said first and second metal layers respectively and having dielectric material in said openings of said first and second metal layers and covering said edges of said first and second metal layers;

(d) forming one or more through vias extending through said coated structure, each said through via being in substantial alignment with said aligned openings in said first and second metal layers;

(e) providing first and second outer metal layers covering said outer dielectric layers;

(f) ~~metalizing~~ metallizing said through vias to form metallic via liners connecting said outer metal layers, and insulated from said first and second metal layers, said dielectric material extending into said vias being disposed between the metallic via liners and said first and second metal layers; and

(g) patterning said outer metal layers such that at least some of said metallic via liners are electrically isolated from said first and second metal layers.

29. (Amended) ~~A~~ The method as claimed in claim 28 ~~further comprising the step of selectively~~ wherein said patterning of said outer metal layers ~~to form~~ forms first signal lines

overlying said first metal layer and second signal lines overlying said second metal layer.

30. (Amended) ~~A~~ The method as claimed in claim 28 further comprising the steps of forming blind vias through said outer dielectric layers to expose one or more regions of said first and second metal layers and metallizing said blind vias so that at least some of said signal lines are connected to some first and second metal layers.

31. (Amended) ~~A~~ The method as claimed in claim 30, wherein the steps of metallizing said through vias and metallizing said blind vias are performed simultaneously.

33. (Amended) ~~A~~ The method as claimed in claim 29, wherein said first signal lines are substantially perpendicular to said second signal lines.

34. (Amended) ~~A~~ The method as claimed in claim 33, wherein the selectively patterning step includes the step of etching the outer metal layers.

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